AMENDMENTS TO THE CLAIMS

1. (currently amended): A coding circuit comprising:

M input lines that receive input signals each including at most one asserted bit, and N output lines that provide binary codes, where M is equal to 2^N; and

for each of the input lines, a set of between zero and N transistors with gates connected to the input line, each of the transistors in the set being connected to change a respective code bit on one of the output lines when turned on by an asserted bit on the input line; while an input line receives an asserted bit, the output lines together providing a respective binary code for the input line; the respective binary codes for the input lines all being unique and between zero and (M−1);

for k=0 to ((M/2)−1), the respective binary codes provided by the output signals for the (2k)th and (2k+1)th input lines being complementary.

2. (original): The circuit of claim 1 in which, for each output line, the transistors that change code bits on the output line are connected in a dynamic OR configuration.

3. (original): The circuit of claim 1 in which the transistors that change code bits on the output lines are NMOS transistors.

4. (original): The circuit of claim 1 in which the input signals indicate locations; the respective binary code of each input line being an address code.

5. (original): The circuit of claim 1 in which M is 16 and N is 4.

6. (original): A signal converter circuit comprising:

first and second sets of lines extending respectively in first and second directions, the first and second directions being different; one of the first and second sets being input lines that receive input signals and the other being output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to one of the input lines; the output signals being converted versions of the input signals; a series of P of the switching elements being connected to one of the second lines and to P consecutive lines in the first set, P being two or more; at least two switching elements in the series having different offsets in the second direction relative to their connected lines in the first set.

7. (original): The circuit of claim 6 in which the lines in the first set are parallel and neighboring lines in the first set are regularly spaced from each other in the second direction by a pitch, the combined effective height of the series of P switching elements being greater than P times the pitch.

8. (original): The circuit of claim 7 in which the combined effective height of the series of P switching elements is approximately 2P times the pitch.

9. (original): The circuit of claim 6 in which P is one of two, three, or four.

10. (original): The circuit of claim 6 in which the offsets are different in direction.

11. (original): The circuit of claim 6 in which the offsets are different in magnitude.

12. (original): The circuit of claim 6 in which the lines in the first set are input lines and the lines in the second set are output lines.

13. (original): The circuit of claim 6 in which each switching element includes a transistor.

14. (original): A signal converter circuit comprising:

input lines that receive input signals;

output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to an asserted input signal on one of the input lines; the switching elements that respond to an asserted input signal on one of the input lines together providing a respective output signal on the output lines that is converted from the asserted input signal; each switching element having at most one neighboring switching element controlling the same output line.

15. (original): The circuit of claim 14 in which one of the switching elements has a neighboring switching element controlling the same output line, the switching element and the neighboring switching element having different offsets in the second direction relative to the input lines to which they respond.

16. (original): The circuit of claim 14 in which each input signal has at most one asserted bit.

17. (original): The circuit of claim 14 in which the respective output signal of each asserted input signal on one of the input lines is complementary with the respective output signal of an asserted input signal on one of the input line's neighboring input lines.

18. (original): A signal converter circuit comprising:

input lines that receive input signals;

output lines that provide, for each of the input signals, a respective code; and

converting circuitry that responds to the input signals, providing the respective codes on the output lines; the converting circuitry responding to assertion of each input line by asserting a respective set of code bits on the output lines; the respective codes bits of each input line being complementary with the respective set of code bits of one of the input line's neighboring input lines.

19. (original): The circuit of claim 18 in which there are M input lines and N output lines, where N is less than M and at least as great as $\log_2 M$.

20. (original): The circuit of claim 18 in which there are M input lines and N output lines, where $N=\log_2 M$.

21. (original): The circuit of claim 18 in which there are M input lines and the respective code of each of the input signals is unique and between zero and (M-1).

22 - 23. (cancel):

24. (original): An encoder circuit comprising:

signal converter circuitry that receives input signals and, in response to each input signal, provides a respective code; the signal converter circuitry providing respective codes that together are a non-ordinal conversion of the input signals; and

recoding circuitry that, in response to each input signal's respective code, provides a recoded code, the recoded codes being an ordinal encoding of the input signals.

25. (original): The circuit of claim 24 in which the input signals are each M-bit signals with one bit asserted and the recoded codes include at least $\log_2 M$ bits, each input signal's respective code being unique and between zero and (M-1).

26. (original): An address converter circuit comprising:

M input lines extending in a first direction, the input lines receiving input signals indicating locations;

N output lines extending in a second direction perpendicular to the first direction, the output lines providing N-bit address codes; N being less than M and at least as great as $\log_2 M$; neighboring input lines being spaced from each other in the second direction by a pitch; and

switching elements, each switching element connected to one of the input lines and one of the output lines; each switching element responding to assertion of its input line by changing the address code bit on its output line;

the switching elements connected to one of the output lines including a pair of neighboring switching elements connected to neighboring input lines; the combined effective height of the pair of neighboring switching elements being greater than twice the pitch; one of the neighboring switching elements having a positive center line offset in the second direction from its connected input line, the other of the neighboring switching elements having a negative center line offset in the second direction from its connected input line.

27. (original): The circuit of claim 26 in which the combined effective height of the pair of neighboring switching elements is approximately 4 times the pitch.

28. (currently amended): An address encoder circuit comprising:

an address converter circuit that receives M-bit input signals indicating locations and, in response to each input signal, provides a respective N-bit address code, where N is less than M and at least as great as $\log_2 M$; each input signal having at most one asserted bit; for k=0 to ($\lfloor M/2 \rfloor - 1$), the respective N-bit address codes for input signals with (2k)th and (2k+1)th bits asserted being complementary; and

a recoding circuit that, in response to each input signal's respective N-bit address code, provides a recoded N-bit address code, the recoded N-bit address codes being an ordinal encoding of the input signals.

29. (currently amended): An address encoder circuit comprising:

an address converter circuit that receives M-bit input signals indicating locations and, in response to each input signal, provides a respective non-ordinal code having N bits, where N is at least $\log_2 M$; each input signal having at most one asserted bit; for k=0 to ($\lfloor M/2 \rfloor - 1$), the input signal with its (2k)th bit asserted having k as its respective non-ordinal code and the input signal with its (2k+1)th bit asserted having the complement of k as its respective non-ordinal code;and

a recoding circuit that, in response to the respective non-ordinal code of each input signal, provides a respective address code having N bits, the least significant bit of each address code being the most significant bit of the respective non-ordinal code; the (N — 1) most significant bits of each address code being:

if the most significant bit of the respective non-ordinal code is "0", the (N —1) least significant bits of the respective non-ordinal code; and

if the most significant bit of the respective non-ordinal code is "1", the complement of the (N —1) least significant bits of the respective non-ordinal code.

30. (currently amended): An address converter circuit comprising:

M parallel, regularly spaced input lines that receive input signals indicating locations and N output lines that provide binary address codes, where M is equal to 2^N; each input signal including at most one asserted bit; neighboring input lines being separated by a pitch;

for each of the input lines, a set of between zero and N NMOS transistors with gates connected to the input line, each of the transistors in the set being connected to pull down a voltage on one of the output lines when turned on by an asserted bit on the input line; while a bit is asserted on an input line, the output lines together providing a respective binary address code for the input line; for k=0 to ($\lfloor M/2 \rfloor - 1$), the input signal with its (2k)th bit asserted having k as its respective non-ordinal code and the input signal with its (2k+1)th bit asserted having the complement of k as its respective non-ordinal code; for each of the output lines, each of the transistors connected to the output line having at most one neighboring transistor connected to the output line; and

for each of the output lines, an output inverter that inverts the voltage on the output line to provide a respective address code bit;

a pair of the transistors being neighboring transistors connected to one of the output lines and with their gates connected to neighboring input lines; the pair of transistors having a combined effective height greater than twice the pitch; the pair of transistors having center lines that are offset differently from their connected input lines.

31. (original): The circuit of claim 30 in which the combined effective height of the pair of transistors is approximately 4 times the pitch.

32. (currently amended): A method of converting signals, comprising:

obtaining M-bit input signals, where M is equal to 2^N; each input signal including at most one asserted bit; and

converting each input signal to a respective N-bit code; the respective N-bit code for each input signal being unique and between zero and (M—1); for k=0 to ($\lfloor M/2 \rfloor$—1), the respective N-bit codes for the input signals with their (2k)th and (2k+1)th bits asserted being complementary.

33. (original): The method of claim 32 in which the input signals indicate locations and the respective N-bit codes are address codes.

34. (cancel):

35. (currently amended): A method of encoding addresses, comprising:

obtaining M-bit input signals indicating locations, each input signal having at most one asserted bit;

converting each input signal to a respective N-bit code, where N is less than M and at least as great as $\log_2 M$; for k=0 to ($\lfloor M/2 \rfloor$—1), the respective N-bit codes for the input signals with their (2k)th and (2k+1)th bits asserted being complementary; and

recoding each input signal's respective N-bit code to an address code with N bits, the address codes being an ordinal encoding of the input signals.

36. (original): The method of claim 35 in which M is equal to 2^N.

37. (currently amended): A method of encoding addresses, comprising:

obtaining M-bit input signals indicating locations, where M is equal to 2^N, each input signal including at most one asserted bit;

converting each input signal to a respective N-bit code; for k=0 to ((M/2)—1), the input signal with its (2k)th bit asserted being converted to an N-bit code with value k and the input signal with its (2k+1)th bit asserted being converted to the complement of the N-bit code with value k; and

recoding the respective N-bit codes to respective address codes with N bits , the least significant bit of each address code being the most significant bit of the respective N-bit code; the (N —1) most significant bits of each address code being:

if the most significant bit of the respective N-bit code is "0", the (N—1) least significant bits of the respective N-bit code; and

if the most significant bit of the respective N-bit code is "1", the complement of the (N—1) least significant bits of the respective N-bit code.

38. (currently amended): An integrated circuit comprising:

a substrate with a surface;

content addressable memory (CAM) circuitry formed at the substrate's surface, including:

a CAM array that stores a set of data items in locations, receives a search data item, and provides, for each location, a match signal indicating whether a data item satisfying a matching criterion is stored in the location;

priority encoder circuitry that, in response to the match signals for the locations, provides an M-bit priority signal with at most one asserted bit, an asserted bit indicating a set of one or more locations in the CAM array for which a match signal indicates that a stored data item satisfies the matching criterion; and

address converter circuitry that, in response to each M-bit priority signal, provides a respective N-bit address code, where N is less than M and at least as great as $\log_2 M$; the respective N-bit address codes together being a non-ordinal encoding of the M-bit priority signals;[[.]] and

a recoder circuitry that, in response to the respective N-bit address code of each M-bit priority signal, provides a recoded N-bit address code; the recoded N-bit address codes of the M-bit priority signals together being an ordinal encoding of the M-bit priority signals.

39. (cancel):

40. (original): The integrated circuit of claim 38 in which the address converter circuitry comprises:

M input lines that receive the priority signals, and N output lines that provide the address codes; and

for each of the input lines, a set of between zero and N transistors with gates connected to the input line, each of the transistors in the set being connected to change a respective address code bit on one of the output lines when turned on by an asserted bit on the input line.

41. (original): The integrated circuit of claim 40 in which, for each output line, the transistors that change code bits on the output line are connected in a dynamic OR configuration.

42. (original): The integrated circuit of claim 40 in which the transistors that change code bits on the output lines are NMOS transistors.

43. (original): The integrated circuit of claim 40 in which one of the transistors has a neighboring transistor connected to the same output line, the transistor and the neighboring transistor having different offsets relative to the input lines to which their gates are connected.

44. (currently amended): The integrated circuit of claim 38 in which, for k=0 to ($\lfloor M/2 \rfloor - 1$), the respective address codes of the priority signals with their (2k)th and (2k+1)th bits asserted are complementary.

45. (original): An integrated circuit comprising:

a substrate with a surface;

content addressable memory (CAM) circuitry formed at the substrate's surface, including:

a CAM array that stores a set of data items in locations, receives a search data item, and provides, for each location, a match signal indicating whether a data item that satisfies a matching criterion is stored in the location;

priority encoder circuitry that, in response to the match signals for the locations, provides an M-bit priority signal with at most one asserted bit indicating a set of one or more locations in the CAM array for which a match signal indicated that a data item satisfied the matching criterion; the priority encoder circuitry including M parallel priority lines on which the M-bit priority signal is provided, the priority lines being uniformly spaced by a first spacing; and

address converter circuitry that, in response to each M-bit priority signal, provides a respective N-bit address code, where N is less than M and at least as great as $\log_2 M$; the address converter circuitry including:

M input lines, each input line being connected to a respective output line from the priority encoder, the input lines being uniformly spaced by approximately the first spacing;

N output lines extending approximately perpendicular to the input lines for providing output signals indicating converted addresses; and

switching elements for converting the priority signals to the output signals, each switching element connected to one of the input lines and one of the output lines; the switching elements connected to one of the output lines including a series of P switching elements connected to P consecutive input lines, P being

two or more; the combined effective height of the P neighboring switching elements being greater than P times the first spacing; at least two of the neighboring switching elements having different offsets relative to their connected input lines.

46. (original): The integrated circuit of claim 45 in which P is equal to two.

47. (original): The circuit of claim 45 in which the combined effective height of the series of P switching elements is approximately 2P times the first spacing.

48. (original): A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including signal converter circuitry that includes:

first and second sets of lines extending respectively in first and second directions, the first and second directions being different; one of the first and second sets being input lines that receive input signals and the other being output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to one of the input lines; the output signals being converted versions of the input signals; a series of P of the switching elements being connected to one of the second lines and to P consecutive lines in the first set, P being two or more;

at least two switching elements in the series having different offsets in the second direction relative to their connected lines in the first set.

49. (original): A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including signal converter circuitry that includes:

input lines that receive input signals;

output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to an asserted input signal on one of the input lines; the switching elements that respond to an asserted input signal on one of the input lines together providing a respective output signal on the output lines that is converted from the asserted input signal; each switching element having at most one neighboring switching element controlling the same output line.

50. (original): A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including signal converter circuitry that includes:

input lines that receive input signals, each having at most one asserted bit;

output lines that provide codes; and

converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines.

51. (cancel):

52. (original): A system comprising:

a processor;

an integrated circuit connected for access by the processor, the integrated circuit including encoder circuitry that includes:

signal converter circuitry that receives input signals and, in response to each input signal, provides a respective code; the signal converter circuitry providing respective codes that together are a non-ordinal conversion of the input signals; and

recoding circuitry that, in response to each input signal's respective code, provides a recoded code, the recoded codes being an ordinal encoding of the input signals.

53. (cancel):

54. (original): A router comprising:

receiving lines that receive data transmissions;

transmitting lines that retransmit data transmissions received on the receiving lines;

CAM circuitry that provides information used to retransmit data transmissions on the transmitting lines, the CAM circuitry comprising signal converting circuitry that includes:

first and second sets of lines extending respectively in first and second directions, the first and second directions being different; one of the first and second sets being input lines that receive input signals and the other being output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to one of the input lines; the output signals being converted versions of the input signals; a series of P of the switching elements being connected to one of the second lines and to P consecutive lines in the first set, P being two or more; at least two switching elements in the series having different offsets in the second direction relative to their connected lines in the first set.

55. (original): A router comprising:

receiving lines that receive data transmissions;

transmitting lines that retransmit data transmissions received on the receiving lines;

CAM circuitry that provides information used to retransmit data transmissions on the transmitting lines, the CAM circuitry comprising signal converting circuitry that includes:

input lines that receive input signals;

output lines that provide output signals; and

switching elements, each switching element controlling one of the output lines in response to an asserted input signal on one of the input lines; the switching elements that respond to an asserted input signal on one of the input lines together providing a respective output signal on the output lines that is converted from the asserted input signal; each switching element having at most one neighboring switching element controlling the same output line.

56. (original): A router comprising:

receiving lines that receive data transmissions;

transmitting lines that retransmit data transmissions received on the receiving lines;

CAM circuitry that provides information used to retransmit data transmissions on the transmitting lines, the CAM circuitry comprising signal converting circuitry that includes:

input lines that receive input signals;

output lines that provide, for each of the input signals, a respective code; and

converting circuitry that responds to the input signals and provides the codes on the output lines; for each input line, the converting circuitry providing a

respective code in response to an asserted bit on the input line; each input line's respective code being complementary with the respective code of one of the input line's neighboring input lines.

57. (cancel):

58. (original): A router comprising:

receiving lines that receive data transmissions;

transmitting lines that retransmit data transmissions received on the receiving lines;

CAM circuitry that provides information used to retransmit data transmissions on the transmitting lines, the CAM circuitry comprising address encoder circuitry that includes:

signal converter circuitry that receives input signals and, in response to each input signal, provides a respective code; the signal converter circuitry providing respective codes that together are a non-ordinal conversion of the input signals; and

recoding circuitry that, in response to each input signal's respective code, provides a recoded code, the recoded codes being an ordinal encoding of the input signals.